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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/804,051	03/12/2001	Salman Akram	MIO 0069 PA/40509.125	7513

23368 7590 11/01/2006

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EXAMINER	
MITCHELL, JAMES M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/804,051	AKRAM ET AL.	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,6-8,25-36,47,49-51,53-57 and 63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,6-8,25-36,47,49-51,53-57 and 63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/20/.2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's request for continued examination filed August 15, 2006.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2, 6, 7, 8, 49, 50 and 57 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear as to the metes and bounds of the limitation "capacitor *accommodated in a space* defined by a *thickness dimension* of a topographic contact". As indicated in a prior office action a plane (x, y etc.) can be extended along any point/component in a package, such that it intersects applicant's contact[1]. The claim is ambiguous in that it could suggest that the capacitor is embedded in the contact. Appropriate correction to clarify applicant's definition is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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[1] The limitation of a capacitor accommodated in a space defined by a thickness dimension of contact is determined to simply mean that the capacitor is equal or less than the height of the contact.

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 6, 7, 25-36, 47, 49-51, 53-58 and 60-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (U.S. 6,507,098) in combination Suzuki et al (US 5,532,910).

6. Lo (Fig. 1) discloses:

(cl. 2, 6, 26, 28, 35, 36, 57) a first [*alternate second* for cl. 31] semiconductor die (26) having a first active surface (i.e. top portion), said first active surface including at least one conductive bond pad (32); a second semiconductor die (40) defining a second active surface (i.e. bottom surface), said second active surface including at least one conductive bond pad (40a); a single intermediate substrate (12) comprising a network of conductive contacts (18) formed thereon, said substrate positioned between said first and second die, such that a first of said intermediate substrate (bottom) faces said first active surface and such that a second surface (top portion) of said intermediate substrate faces said second active surface (bottom portion), said intermediate substrate includes a passage (defined by item 24) and one of the first and second die active surface aligned with the passage (i.e. die, 26), a printed circuit board (100) positioned such that a first surface (i.e. top portion) of the board faces the intermediate substrate; a plurality of topographic contacts (48) extending from said intermediate substrate to said first surface of said board;

(25) wherein said first die is electrically connected to the intermediate substrate by a topographic contact (52) extending from said first active surface to said intermediate

with said second die secured (34) to the second surface of the intermediate substrate, such that the conductive pads (32) of the second die is aligned with the passage and said second die is electrically connected to the intermediate substrate by at least one conductive line (38) extending from the bond pad of the second die through said passage and to contact first surface of the intermediate substrate;

(cl. 27, 29) and the second/ *first* chip (40, 42) is flip is stacked secured to first surface of intermediate substrate (22);

(cl. 30-32) with conductive lines extending from pad (14) on the intermediate substrate to pads on active areas (i.e. chip connection to pads by pads/ or wire);

(cl. 33) die further electrically connected to intermediate substrate (i.e. chip connection to pads by pads/ or wire);

(cl. 34) and the first die is electrically connected to the second die (i.e. both in communication with external contact, 48);

(cl. 54, 55) with the intermediate substrate includes a network of contacts formed thereon (i.e. 14);

(cl. 63) a passage substantially free of encapsulant (e.g. intermediate structure prior to chip being enveloped by encapsulant; Col. 4, Lines 9-20).

7. Lo does not discloses at least one decoupling capacitor mounted to a first surface of an intermediate substrate and conductively coupled to at least one of said first and second semiconductor dies or wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of

one of said first semiconductor die, said second semiconductor die, or a topographic contact.

8. Suzuki utilizes a decoupling capacitor accommodated in a space, mounted on an intermediate substrate and coupled to a die Suzuki (Col. 1, Lines 48).

9. It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor into the modified package including Lo in order to remove noise as taught by Suzuki (Col. 1, Lines 48).

10. With respect to the placement of the capacitor, such that it is mounted on the intermediate substrate, or that a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor[1], it would have been obvious, since the rearrangements of parts have been held unpatentable absent a showing of criticality or unexpected results. *See e.g. In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) (claims held unpatentable because shifting the position of the starting switch would not have modified the operation of the device); see also *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

11. With respect to the claims 7, 49 and 50 and their dependents regarding the mere duplication of an element (i.e. intermediate substrate), since applicant has not disclosed that the duplication is for a new and unexpected result, the limitation has no patentable significance. See In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960) (Although

the reference did not disclose a plurality of ribs, the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced).

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (U.S. 6,507,098) in combination with Distefano (U.S. 6,075,289), Suzuki et al (US 5,532,910) and Searls (U.S. 2004/0155335).

13. Lo (Fig. 1) discloses the elements stated in paragraph 6 of this office action[2], but does not discloses a cap including a heat sink coupled to at least one die major surface with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate, or at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies or wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, or a topographic contact, or connecting capacitor between high and low voltage inputs.

14. Distefano (Fig. 2) discloses a cap including a heat sink coupled to at least one die major surface (i.e. horizontal surface) with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate.

15. It would have been obvious to one of ordinary skill in the art to incorporate a cap including a heat sink to package of Lo in order to provide thermally enhanced packages as taught by Distefano (Title).

16. Suzuki utilizes a decoupling capacitor accommodated in a space coupled to a die Suzuki (Col. 1, Lines 48).

17. It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor into the modified package including Lo in order to remove noise as taught by Suzuki (Col. 1, Lines 48). Moreover with respect to placement being in a thickness dimensions, see paragraph 12 of this office action.

18. Neither Lo, Distefano or Suzuki disclose attaching a capacitor between high and low voltages.

19. However Searls (Fig. 1; Par. 0067) utilizes disclose attaching a capacitor (130) between high and low voltages (118,140).

20. It would have been obvious to one of ordinary skill in the art to connect the modified package of Lo to include attaching a capacitor between high an low voltages in order to improve device performance as taught by Searls (Abstract).

Response to Arguments

21. Besides the rejection based on claim 8[3], applicant's arguments filed April 11, 2006 have been fully considered, but they are not persuasive. The gravamen of applicant's argument is that examiner has provided no motivation for rearrangement of a capacitor quoting from *Ex parte Chicago Rawhide Manufacturing Company* that " The

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[2] Since applicant can be their own lexicographer the first and second surfaces are interchanged. For example, claim two's second semiconductor die (40) is first die for claim 8, and alternatively the first surface of the intermediate substrate (e.g. bottom) is the second surface for claim 8.
[3] New rejection provided to address limitation.

mere fact that a worker in the art could rearrange the parts...not by itself sufficient to support a finding of obviousness...."

22. While applicant is correct that the mere ability to rearrange is not sufficient to support obviousness; he has failed to recognize that this is based on situations where the movement creates functional changes.[4] This distinction is highlighted by the courts comments in dictum that "the relative movements of the various elements ...would not be met...even if reconstructed as suggested by the ...examiner." *Ex parte Chicago Rawhide Manufacturing Co.,* 223, USPQ 351, 353 (Bd. Pat. App. & Inter. 1984). Absent extrinsic evidence to the contrary, because movement of the capacitor within a package would not have modified the operation of the device or resulted in unexpected results, applicant's arguments are found unpersuasive.

23. As for applicant's allegation of no motivation, because none of the references allegedly show the claimed feature or provide a motivation for the claimed placement of the capacitor, a showing of the claimed feature or an explicit motivation is not needed. The prior art in a 103 obviousness-type rejection need not show/anticipate a claim, but rather legal precedent can provide the rational supporting obviousness of the modification. *See* M.P.E.P 2144[R-5]. In this instance, it has been held that mere rearrangement of parts is prima facie obviousness absent a showing of criticality or unexpected results[5]. For the reasons stated above, applicant's arguments are found unpersuasive.

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[4] In addition, the board is administrative court and must follow the precedent set before it. See for e.g. *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950). The interpretation suggested by applicant would be inconsistent with precedent.

[5] Id.

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ex. Mitchell, J.D.
October 29, 2006

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800